IN THE SPECIFICATION

Please amend the paragraph beginning on page 13 line 4 as follows:

As shown in FIG. 5F, the remaining nitride layer 322 exposed in openings 326 is directionally etched to expose layer of intrinsic poly-silicon 320. It is noted that nitride layer 322 and nitride layer 310 remain intact under the photo resist layer 324. Layer of intrinsic poly-silicon 320 is next isotropically etched using a silicon etchant which does not attack oxide or nitride layers. Next, an isotropic oxide etch is performed to remove all exposed thin oxide. The photo resist layer 324 is removed. At this point, the method has produced the structure shown in FIG. 5G. This structure includes a nitride bridge formed from nitride layers 310 and 322 that extends orthogonal to column isolation trenches 316 and covers the remaining portions of layers 302, 304, and 306. The structure also includes row isolation trenches [[322]] 332 that are orthogonal to column isolation trenches 316. The structure of FIG. 5G also includes pillars 334A through 334D of single crystal silicon material. Pillars 334A through 334D form the basis for individual memory cells for the memory array formed by the process.

Please amend the paragraph beginning on page 13 line 26 as follows:

Next, a common plate for all of the memory cells of array 299 is formed by a chemical vapor deposition of N+ poly-silicon or other appropriate refractory conductor in column isolation trenches 316 and row isolation trenches [[322]] 332. In this manner, conductor mesh or grid 340 is formed so as to surround each of pillars 334A through 334D. Mesh 340 is planarized and etched back to a level approximately at the bottom of the nitride bridge formed by nitride layers 322 and 310 as shown in FIG. 5H. An additional etch is performed to remove any remaining exposed capacitor dielectric of layer 338 from the sides of semiconductor pillars 334A through 334D.